

FIG. 1

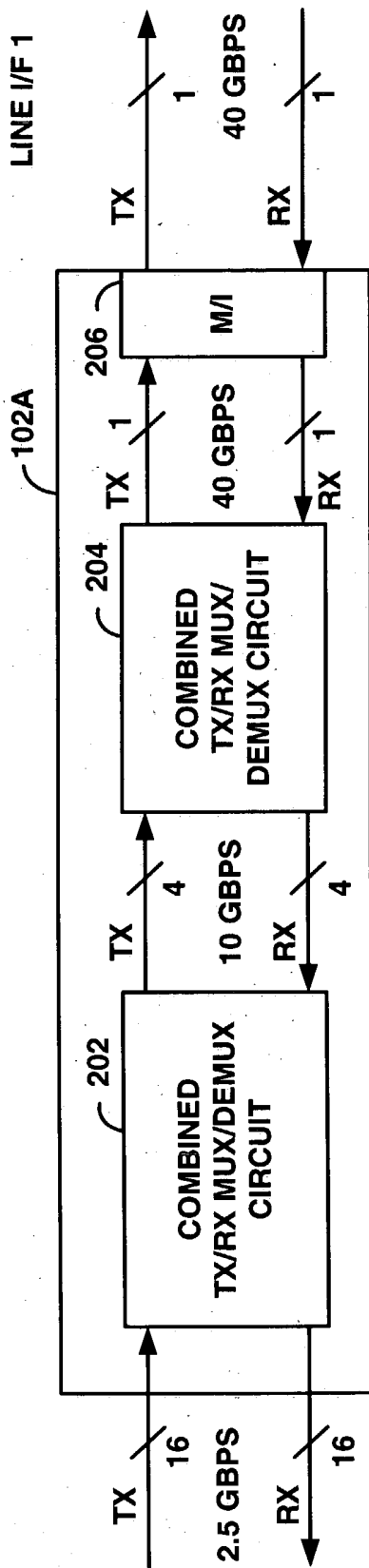


FIG. 2A

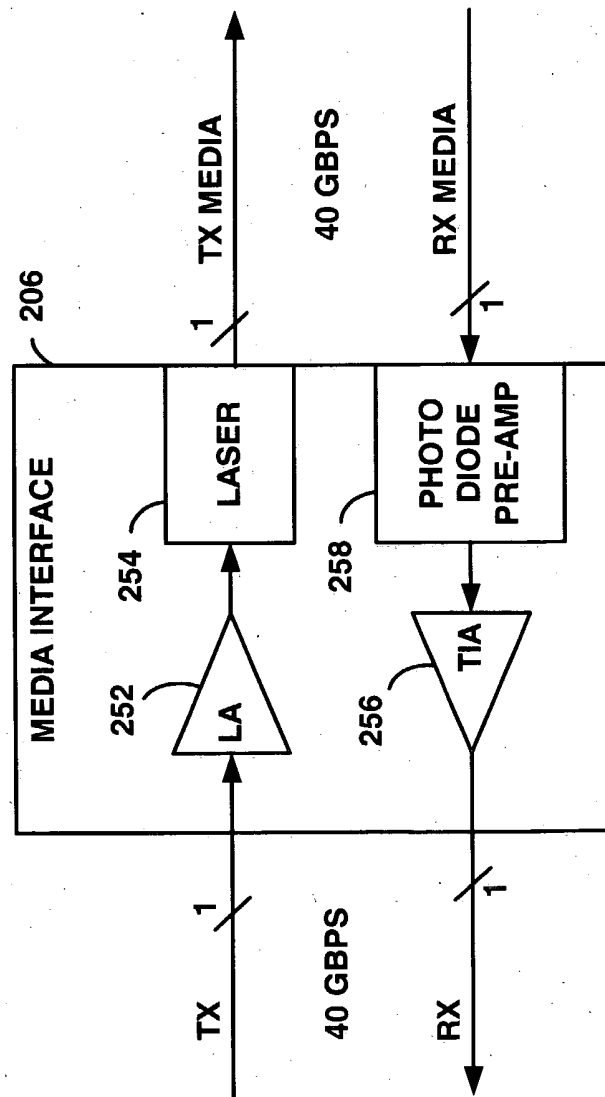


FIG. 2B

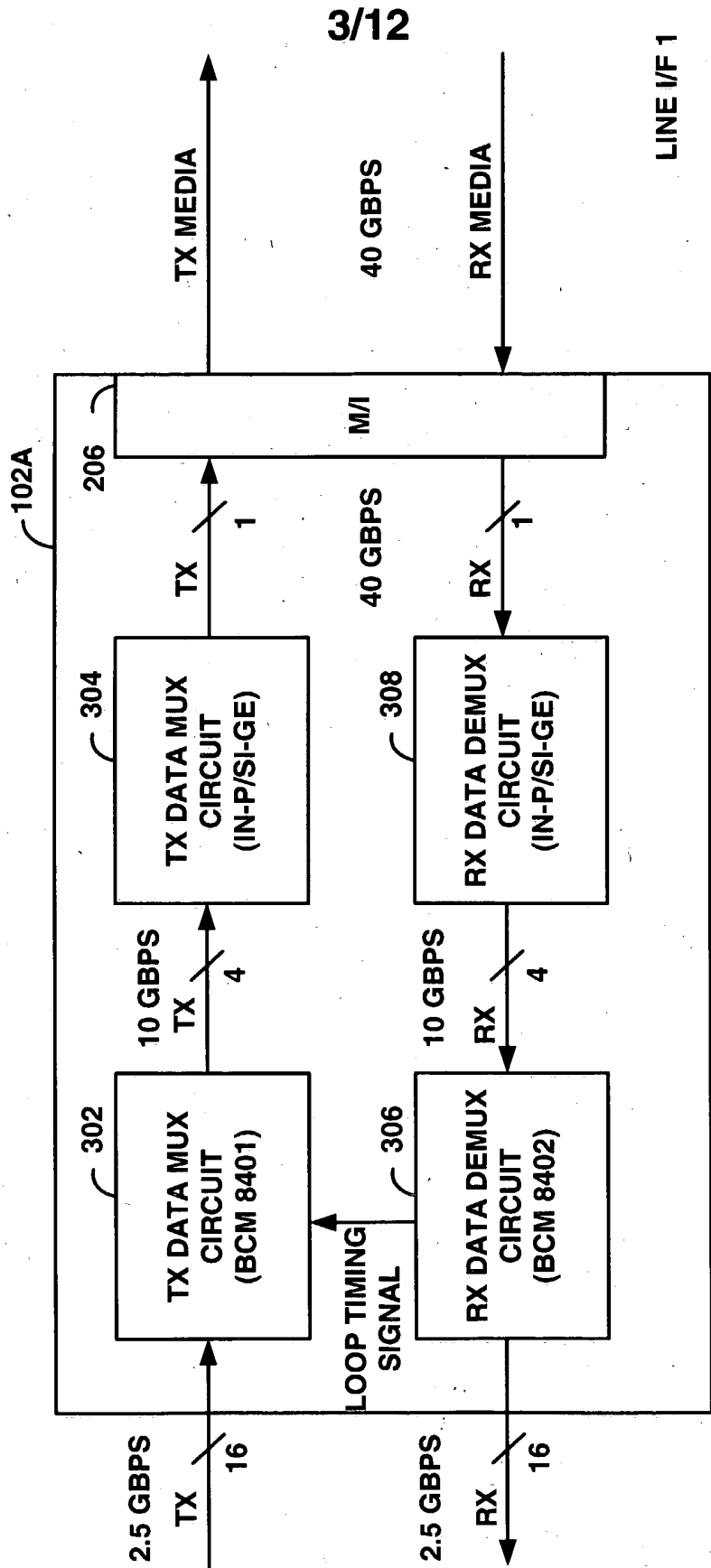


FIG. 3

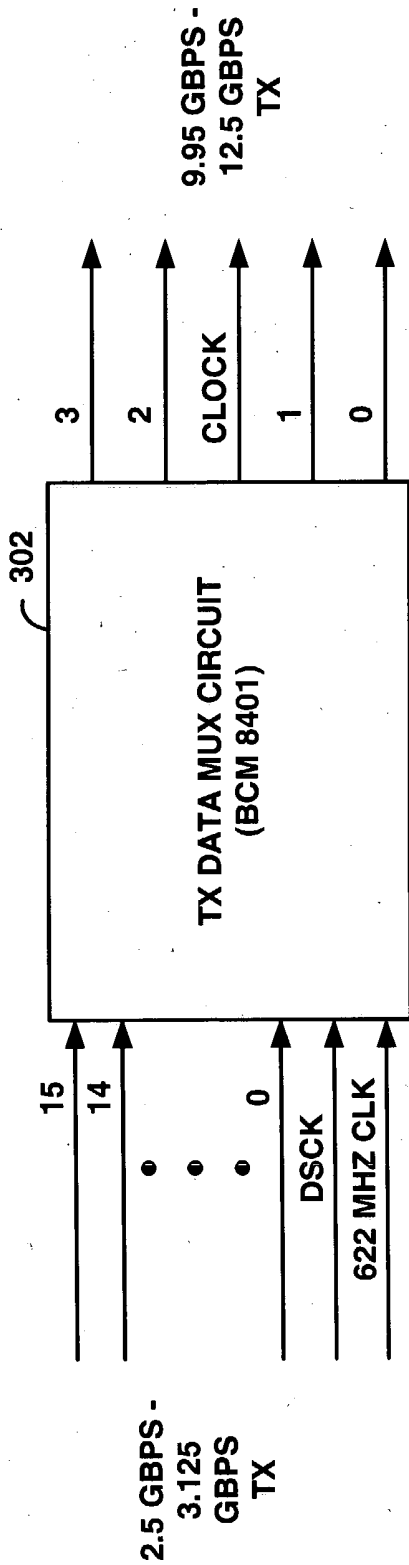


FIG. 4A

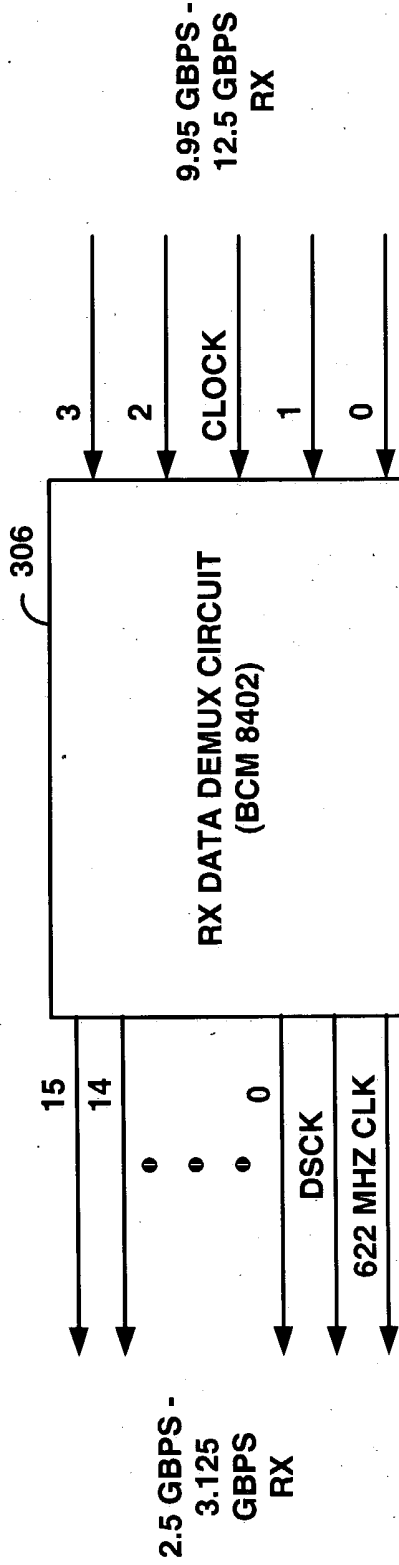


FIG. 4B

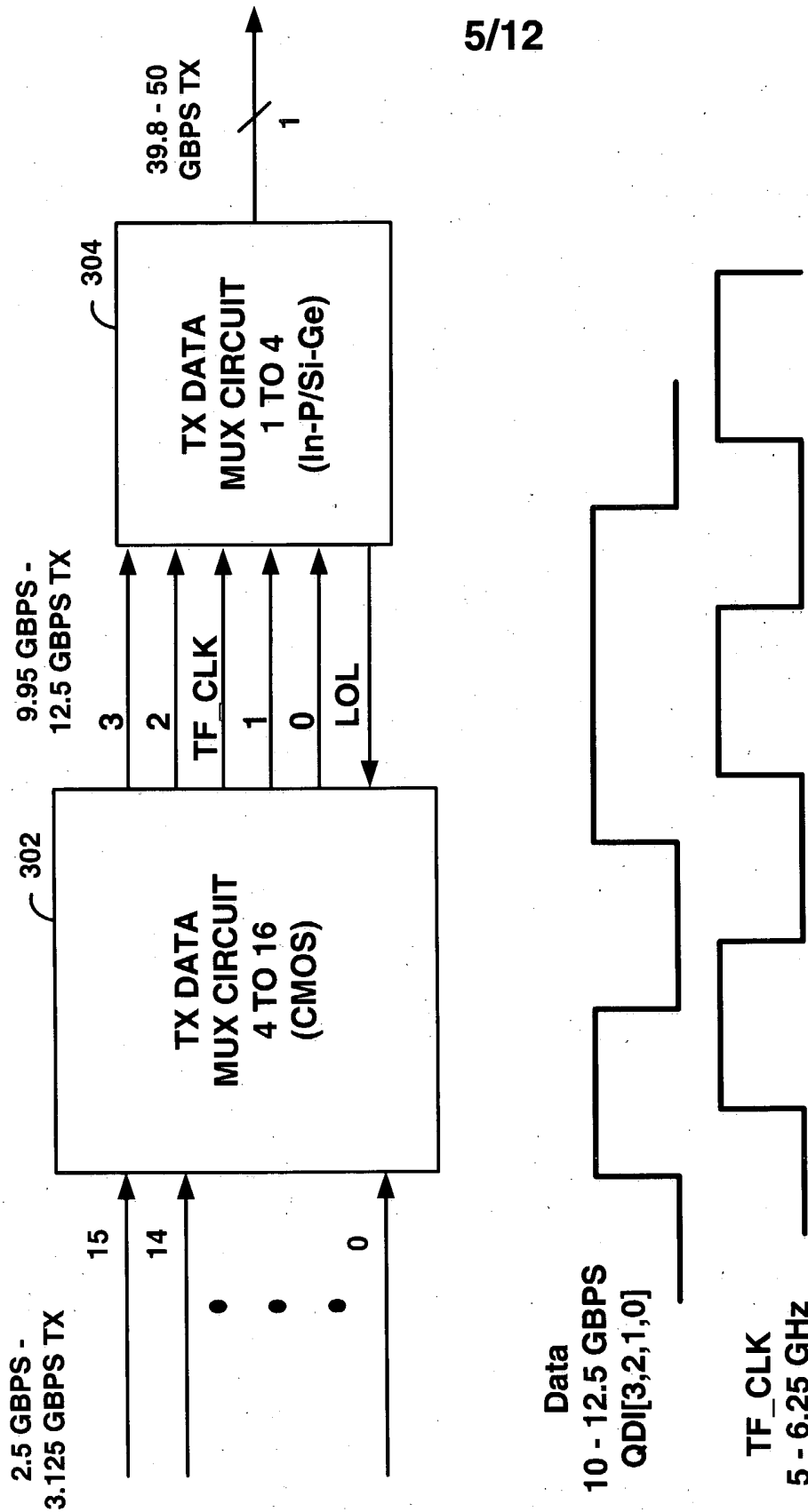


FIG. 5

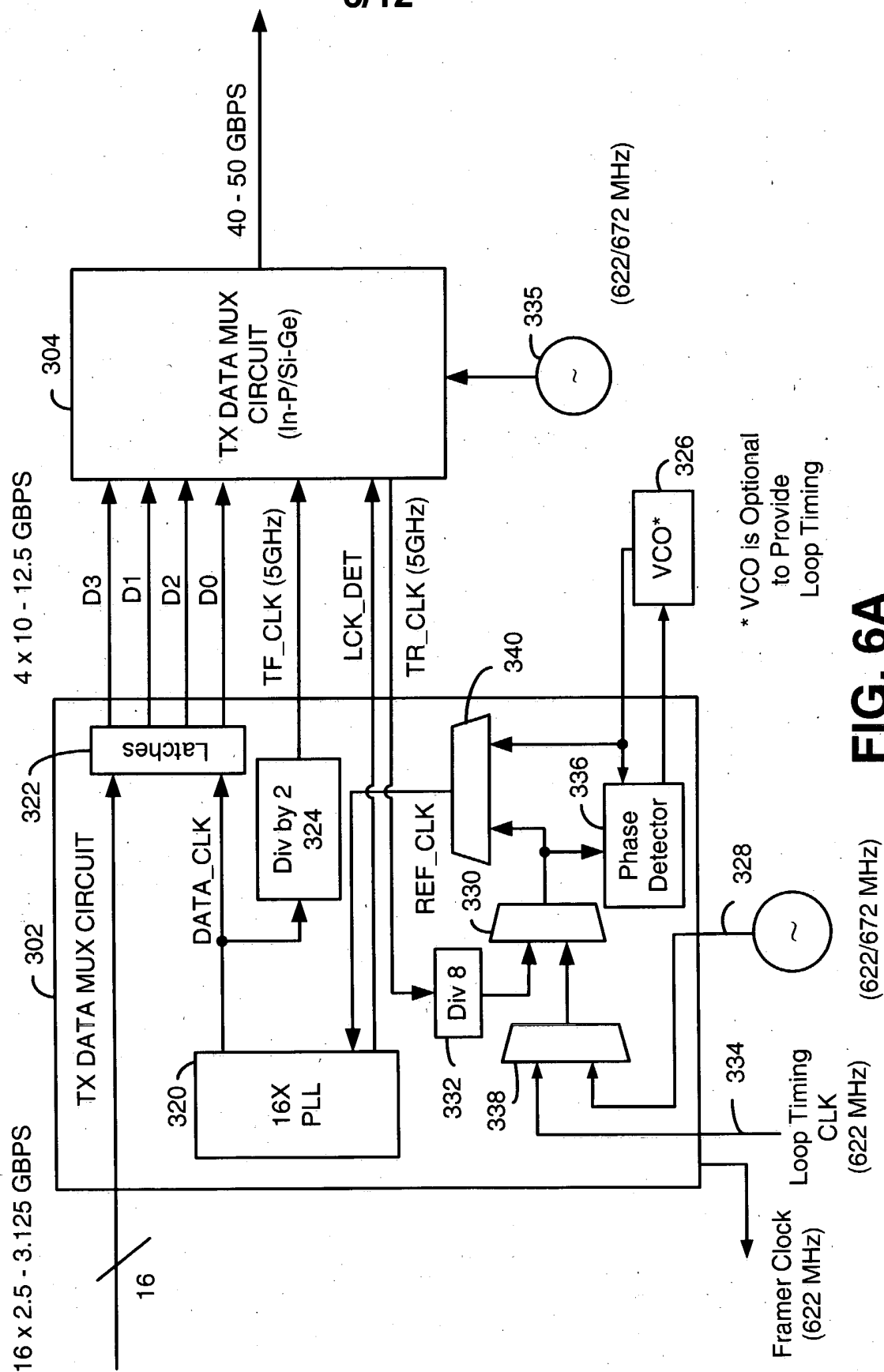


FIG. 6A

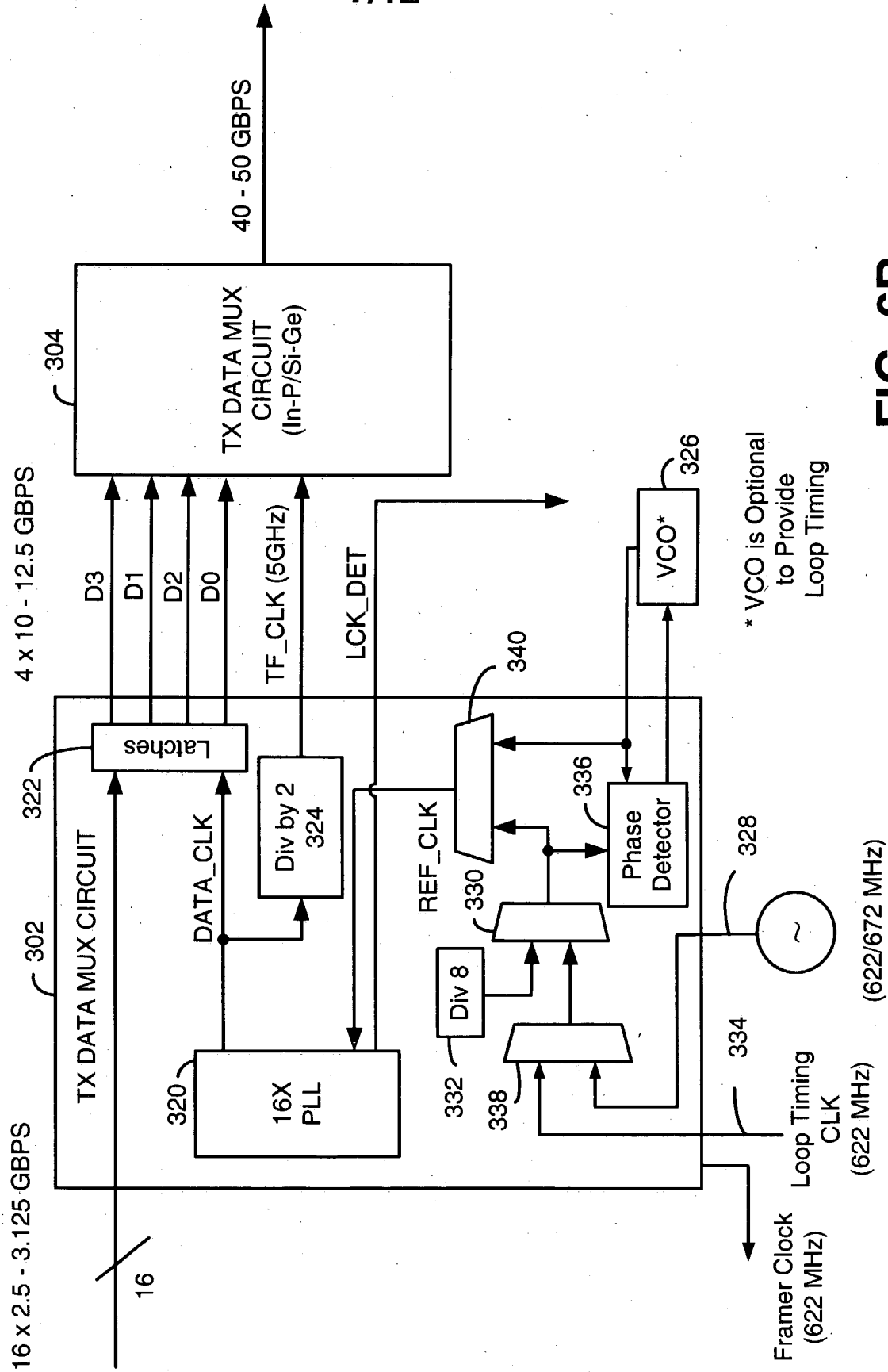


FIG. 6B

Receiver Input and Source Centered Clock Performance

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output Common Mode	V_{cm}	See Figure Below	1575	1675	1775	mV
Single Ended Output Impedance	Z_{SE}		40	50	60	Ω
Differential Input impedance	Z_d		80	100	120	Ω
Input Impedance Mismatch	Z_M				10	%
Q40, CML Input Differential Amplitude, p-p	ΔV_{QDO}	See Figure Below	400	500	600	mV
Q40 Input Rise and Fall Time (20% to 80%)	t_{RH}, t_{FH}			25	35	ps
Differential output return loss*	S11	Up to 7.5 GHz	10			dB
4-by-1 mux input return loss > 15 db at 10 GHz						

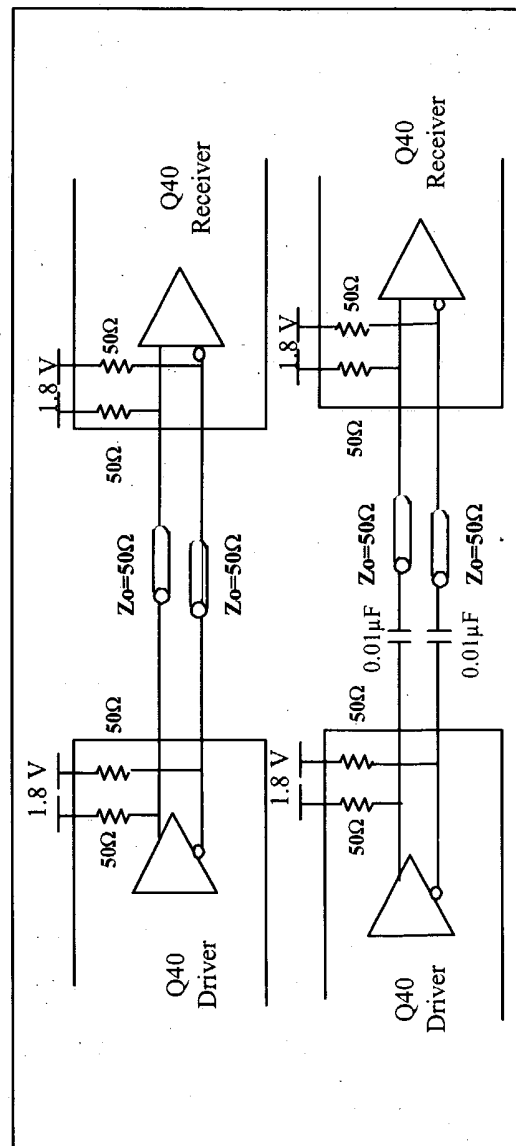


FIG. 7

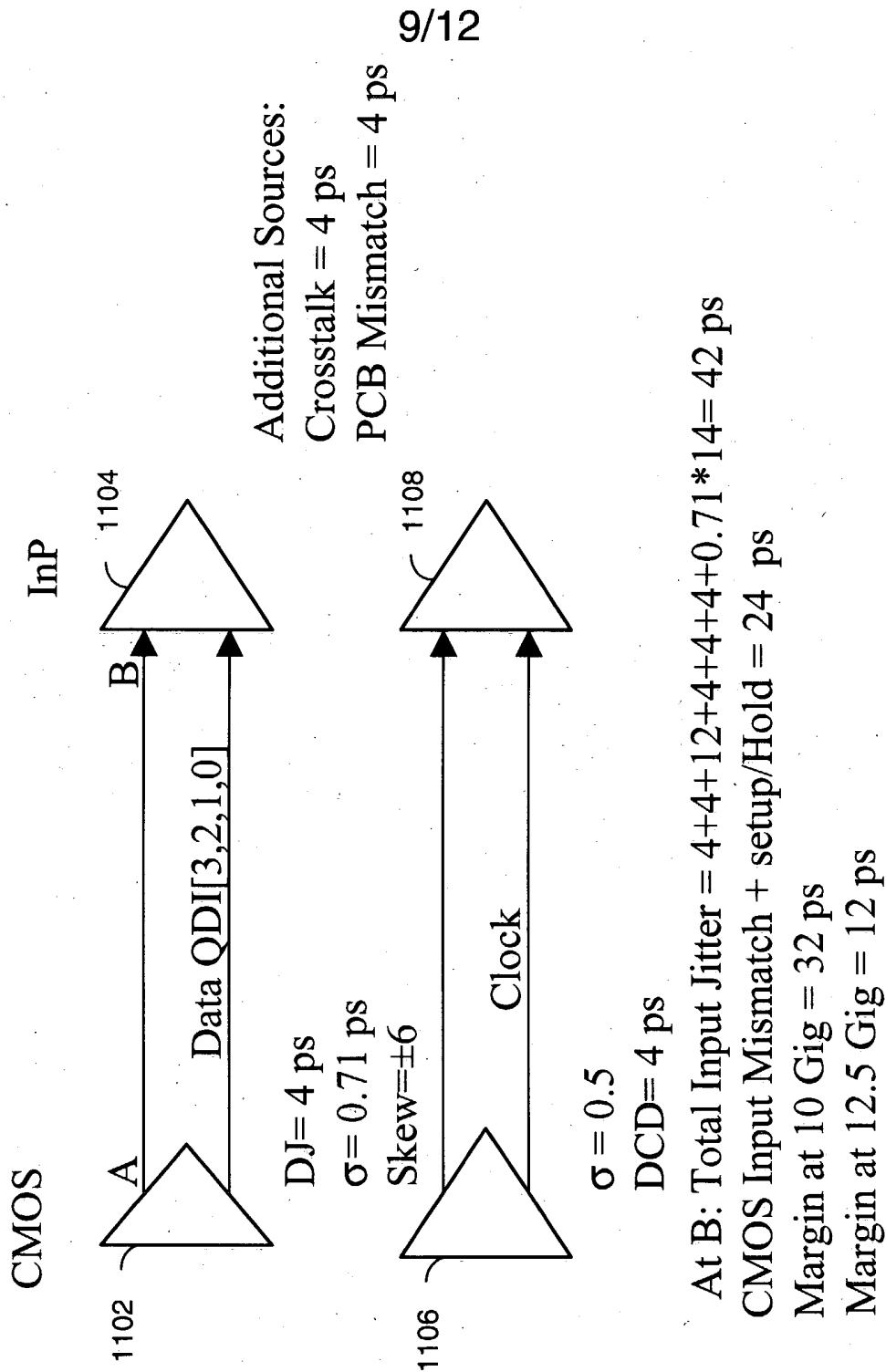


FIG. 8

Transmit and Receive

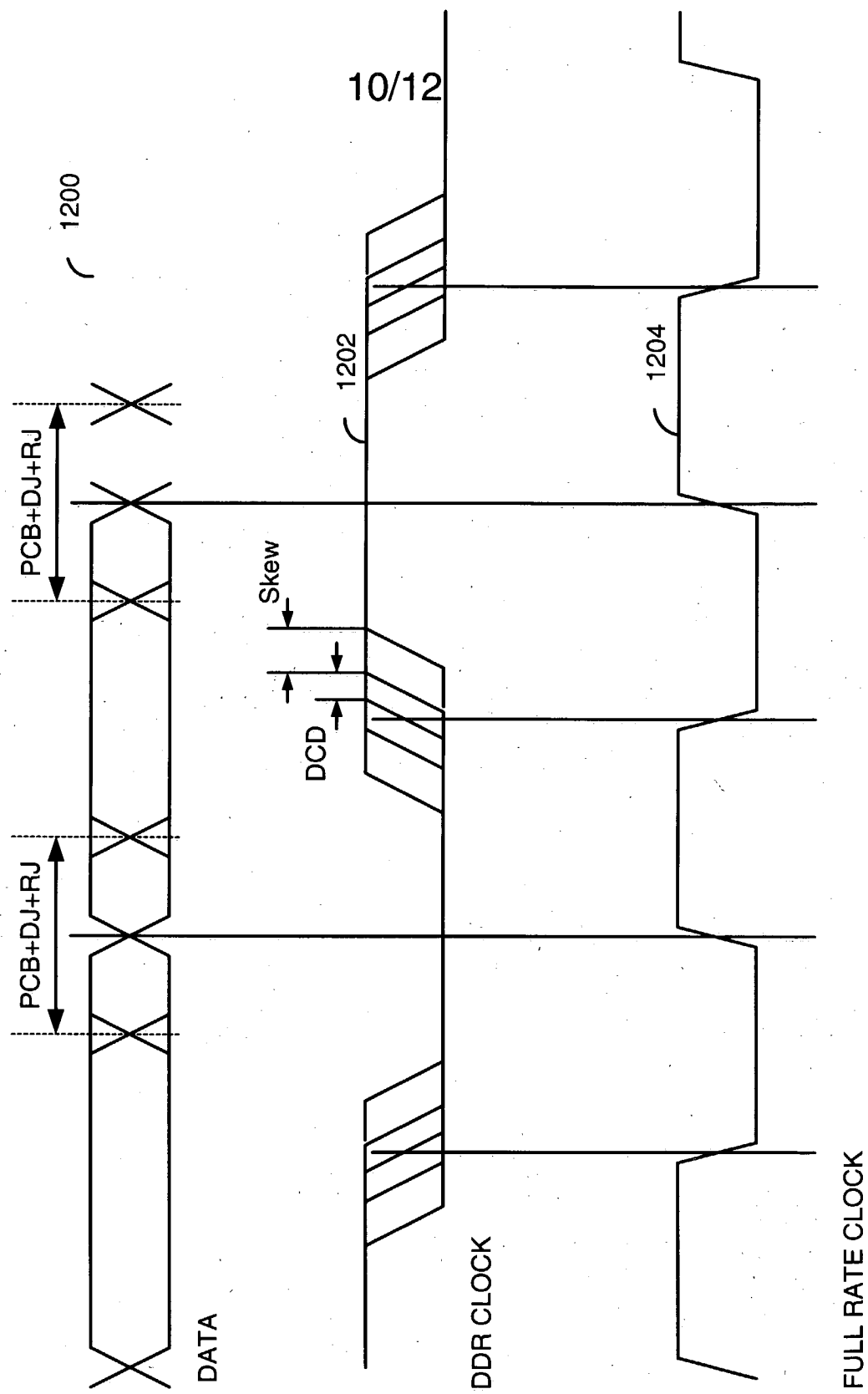


FIG. 9

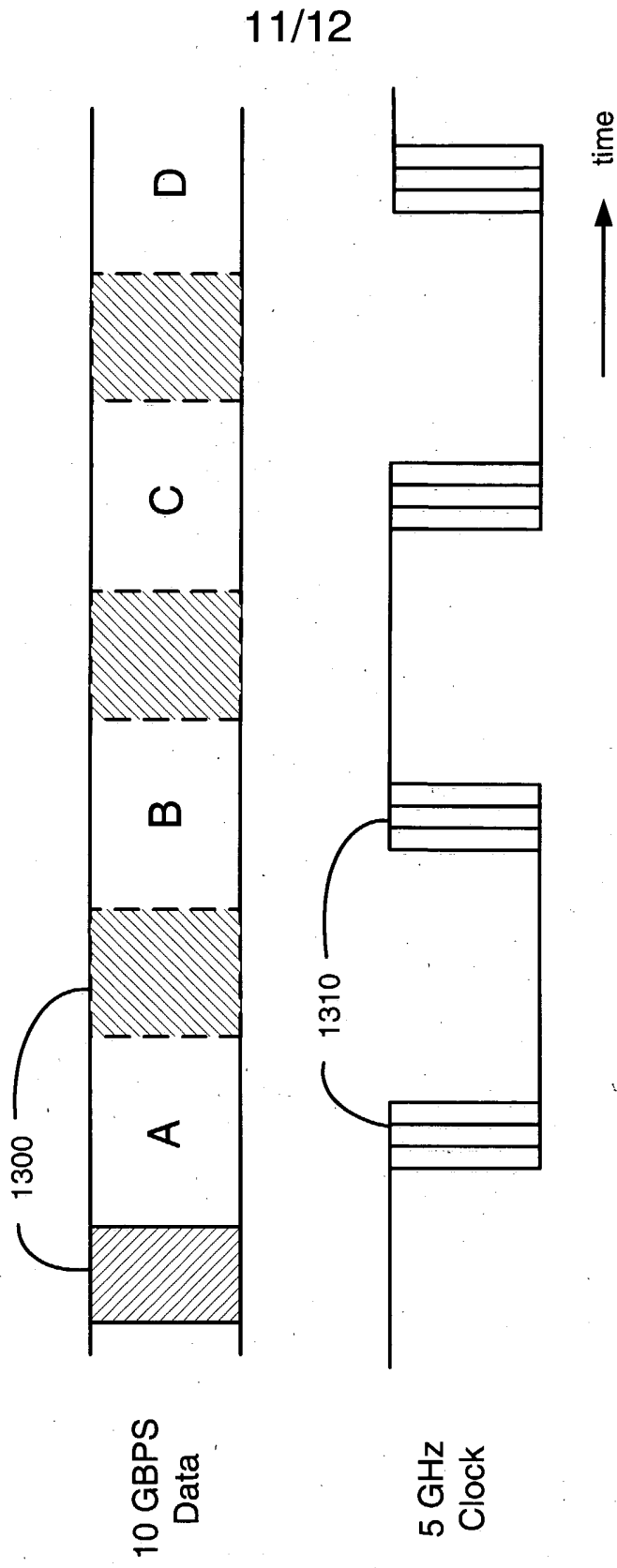
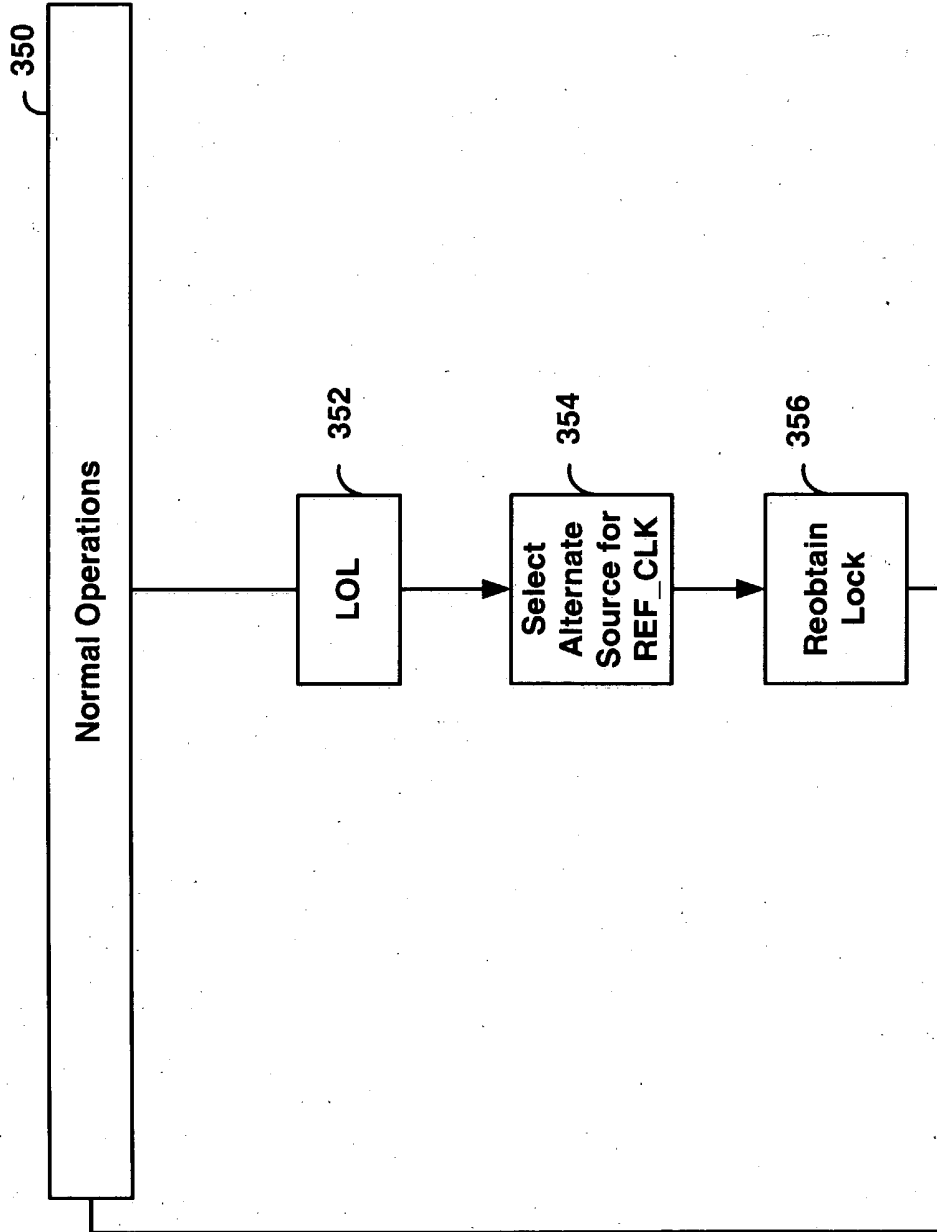


FIG. 10

**FIG. 11**